Clock outputs
The top jack outputs a positive polarity gate, *(rising on the clock division)*.

The lower jack flips the polarity to step between divisions: *(falling on the clock division, rising between divisions)*.

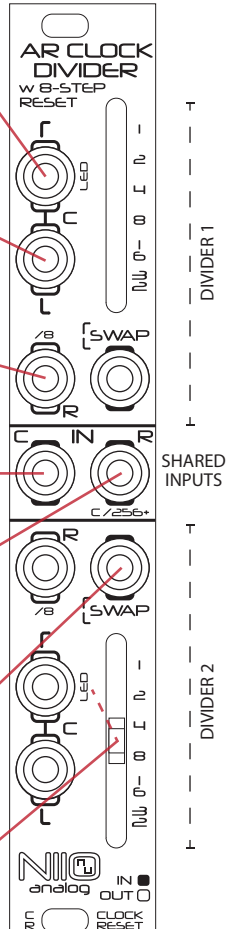
Reset output
Outputs a gate on the 1st step every cycle.

Clock input
A 50/50 duty cycle gate is preferred for /1 inverse output.

Reset input
A gate input resets both dividers. Should be the clock divided by 256 steps or greater for /32.

Swap input
A gate swaps the polarity of both outputs.

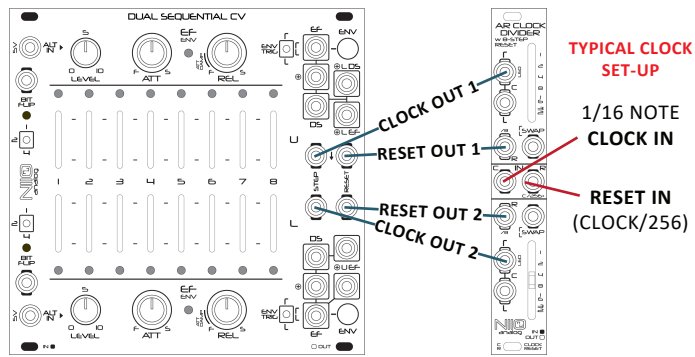
Division slider
Sets the division from /1 to /32.
The LED illuminates with the divided clock and mirrors the top clock output jack.



AUTO RESET
analog clock divider

8 - STEP SEQUENCER

AR CLOCK DIVIDER



PATCHING EXAMPLE

width: 4hp depth: 37mm 12ma +12v